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Mayer, A.;
Proceedings of the IEEE
Volume 55, Issue 8, Aug. 1967 Page(s):1502 - 1504
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3. **Thermal radio radiation from the moon and planets**
Mayer, C.;
Antennas and Propagation, IEEE Transactions on [legacy, pre - 1988]
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4. **Feed region modes in dipole phased arrays**
Mayer, E.; Hessel, A.;
Antennas and Propagation, IEEE Transactions on [legacy, pre - 1988]
Volume 30, Issue 1, Jan 1982 Page(s):66 - 75
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5. **Line-of-sight observations at 86 GHz with a very large and a small antenna**
Vogel, W.; Davis, J.; Mayer, C.;
Antennas and Propagation, IEEE Transactions on [legacy, pre - 1988]
Volume 32, Issue 2, Feb 1984 Page(s):113 - 118
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6. **A design procedure for dielectric microwave lenses of large aperture ratio and large scanning angle**
Holt, F.; Mayer, A.;
Antennas and Propagation, IEEE Transactions on [legacy, pre - 1988]
Volume 5, Issue 1, Jan 1957 Page(s):25 - 30
AbstractPlus | Full Text: PDF(512 KB) **IEEE JNL**

7. **Correction to "A design procedure for dielectric microwave lenses of large aperture ratio and large scanning angle"**
Holt, F.; Mayer, A.;
Antennas and Propagation, IEEE Transactions on [legacy, pre - 1988]

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☐ **1. Comparison of simulation algorithms for accelerated determination of periodic steady state of switched networks**
Duwang L; Tymerski, R.;
Industrial Electronics, IEEE Transactions on
Volume 47, Issue 6, Dec. 2000 Page(s):1278 - 1285
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☐ **2. Simulations of racetrack microtron for acceleration of picosecond electron pulse**
Washio, M.; Kuroda, R.; Yang, J.; Hori, T.; Sakai, F.;
Particle Accelerator Conference, 1999. Proceedings of the 1999
Volume 4, 27 March-2 April 1999 Page(s):2298 - 2300 vol.4
Digital Object Identifier 10.1109/PAC.1999.792667
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Ellis-Monaghan, J.J.; Hulfachor, R.B.; Kim, K.W.; Littlejohn, M.A.;
Electron Devices, IEEE Transactions on
Volume 43, Issue 7, July 1996 Page(s):1123 - 1132
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Bin-Hong Lin; Shao-Hui Shieh; Cheng-Wen Wu;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 19, Issue 9, Sept. 2000 Page(s):1031 - 1040
Digital Object Identifier 10.1109/43.863643
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Shvetsov, G.A.; Stankevich, S.V.;
Magnetics, IEEE Transactions on
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Digital Object Identifier 10.1109/TMAG.2002.806422
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Albrecht P. Stroele, Frank **Mayer**: Methods to reduce test application time for ... **Microprocessor** Test and Validation: Any New Avenues? 458-464 ...
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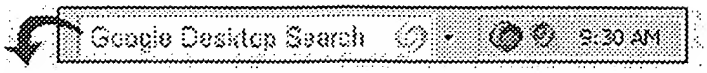

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1 Trace-driven memory simulation: a survey

Richard A. Uhlig, Trevor N. Mudge

June 1997 **ACM Computing Surveys (CSUR)**, Volume 29 Issue 2

Publisher: ACM Press

Full text available: pdf(636.11 KB) Additional Information: full citation, abstract, references, citings, index terms, review

As the gap between processor and memory speeds continues to widen, methods for evaluating memory system designs before they are implemented in hardware are becoming increasingly important. One such method, trace-driven memory simulation, has been the subject of intense interest among researchers and has, as a result, enjoyed rapid development and substantial improvements during the past decade. This article surveys and analyzes these developments by establishing criteria for evaluating trac ...

Keywords: TLBs, caches, memory management, memory simulation, trace-driven simulation

2 Functional verification methodology of Chameleon processor

Françoise Casaubieilh, Anthony McIsaac, Mike Benjamin, Mike Bartley, François Pogodalla, Frédéric Rocheteau, Mohamed Belhadj, Jeremy Eggleton, Gérard Mas, Geoff Barrett, Christian Berthet

June 1996 **Proceedings of the 33rd annual conference on Design automation**

Publisher: ACM Press

Full text available: pdf(62.38 KB) Additional Information: full citation, references, citings, index terms

3 Special section: Reasoning about structure, behavior and function

B. Chandrasekaran, Rob Milne

July 1985 **ACM SIGART Bulletin**, Issue 93

Publisher: ACM Press

Full text available: pdf(5.13 MB) Additional Information: full citation, abstract, references

The last several years' of work in the area of knowledge-based systems has resulted in a deeper understanding of the potentials of the current generation of ideas, but more importantly, also about their limitations and the need for research both in a broader framework as well as in new directions. The following ideas seem to us to be worthy of note in this connection.

4 Design of heterogeneous ICs for mobile and personal communication systems

Gert Goossens, Ivo Bolsens, Bill Lin, Francky Catthoor

November 1994 **Proceedings of the 1994 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Computer Society Press

Full text available: pdf(1.04 MB) Additional Information: full citation, abstract, references, citings, index terms

Mobile and personal communication systems form key market areas for the electronics industry of the nineties. Stringent requirements in terms of flexibility, performance and power dissipation, are driving the development of integrated circuits into the direction of heterogeneous single-chip solutions. New IC architectures are emerging which contain the core of a powerful programmable processor, complemented with dedicated hardware, memory and interface structures. In this tutorial we will d ...

5 Hardware/software co-simulation in a VHDL-based test bench approach

Matthias Bauer, Wolfgang Ecker

June 1997 **Proceedings of the 34th annual conference on Design automation - Volume 00**

Publisher: ACM Press

Full text available: pdf(88.32 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Novel test bench techniques are required to cope with afunctional test complexity which is predicted to grow muchmore strongly than design complexity. Our test benchapproach attacks this complexity by using a stronghierarchical architecture, application domain-independentsynchronization, reusable modules, and easy incrementalextendability based on table-driven techniques. In addition,the integration of VHDL/C co-simulation under the controlof the test bench makes it possible to use the hardware ...

6 Human-computer interface development: concepts and systems for its management

H. Rex Hartson, Deborah Hix

March 1989 **ACM Computing Surveys (CSUR)**, Volume 21 Issue 1

Publisher: ACM Press

Full text available: pdf(7.97 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Human-computer interface management, from a computer science viewpoint, focuses on the process of developing quality human-computer interfaces, including their representation, design, implementation, execution, evaluation, and maintenance. This survey presents important concepts of interface management: dialogue independence, structural modeling, representation, interactive tools, rapid prototyping, development methodologies, and control structures. *Dialogue independence* is th ...

7 Realizing OpenGL: two implementations of one architecture

Mark J. Kilgard

August 1997 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**

Publisher: ACM Press

Full text available: pdf(1.66 MB) Additional Information: full citation, references, citings, index terms

Keywords: O2, OpenGL, graphics hardware architecture, infinite-reality

8 Launching the new era

Kazuhiro Fuchi, Robert Kowalski, Koichi Furukawa, Kazunori Ueda, Ken Kahn, Takashi Chikayama, Evan Tick

March 1993 **Communications of the ACM**, Volume 36 Issue 3

Publisher: ACM Press

Full text available: pdf(3.45 MB) Additional Information: full citation, references, index terms, review

9 Tempest and typhoon: user-level shared memory

S. K. Reinhardt, J. R. Larus, D. A. Wood

April 1994 **ACM SIGARCH Computer Architecture News , Proceedings of the 21ST annual international symposium on Computer architecture ISCA '94**, Volume 22 Issue 2

Publisher: IEEE Computer Society Press, ACM Press

Full text available: pdf(1.44 MB) Additional Information: full citation, abstract, references, citings, index terms

Future parallel computers must efficiently execute not only hand-coded applications but also programs written in high-level, parallel programming languages. Today's machines limit these programs to a single communication paradigm, either message-passing or shared-memory, which results in uneven performance. This paper addresses this problem by defining an interface, *Tempest*, that exposes low-level communication and memory-system mechanisms so programmers and compilers can customize polici ...

10 The space shuttle primary computer system

Alfred Spector, David Gifford

September 1984 **Communications of the ACM**, Volume 27 Issue 9

Publisher: ACM Press

Full text available: pdf(5.34 MB) Additional Information: full citation, references, citings, index terms

Keywords: PASS, avionics system, space shuttle

11 Special issue: AI in engineering

D. Sriram, R. Joobbani

April 1985 **ACM SIGART Bulletin**, Issue 92

Publisher: ACM Press

Full text available: pdf(8.79 MB) Additional Information: full citation, abstract

The papers in this special issue were compiled from responses to the announcement in the July 1984 issue of the SIGART newsletter and notices posted over the ARPAnet. The interest being shown in this area is reflected in the sixty papers received from over six countries. About half the papers were received over the computer network.

12 Rapid simulation of wireless systems

L. Felipe Perrone, David M. Nicol

July 1998 **ACM SIGSIM Simulation Digest , Proceedings of the twelfth workshop on Parallel and distributed simulation PADS '98**, Volume 28 Issue 1

Publisher: IEEE Computer Society, ACM Press

Full text available: pdf(1.02 MB) Publisher Site Additional Information: full citation, references, citings, index terms

13 PACS: a parallel microprocessor array for scientific calculations

Tsutomu Hoshino, Toshio Kawai, Tomonori Shirakawa, Junchi Higashino, Akira Yamaoka, Hachidai Ito, Takashi Sato, Kazuo Sawada

August 1983 **ACM Transactions on Computer Systems (TOCS)**, Volume 1 Issue 3

Publisher: ACM Press

Full text available: pdf(1.95 MB) Additional Information: full citation, references, citings, index terms

Keywords: MIMD, array processors, distributed systems, highly parallel processors, multimicroprocessors, multiprocessing, multiprocessors, nearest neighbor communication, parallel algorithms, parallel language, parallel processors, performance measurement, processor architecture, scientific calculation, supercomputer, synchronization

14 Tempest and typhoon: user-level shared memory

Steven K. Reinhardt, James R. Larus, David A. Wood

August 1998 **25 years of the international symposia on Computer architecture (selected papers)**

Publisher: ACM Press

Full text available: pdf(1.57 MB) Additional Information: full citation, references, index terms

15 An empirical evaluation of two memory-efficient directory methods

Brian W. O'Krafka, A. Richard Newton

May 1990 **ACM SIGARCH Computer Architecture News , Proceedings of the 17th annual international symposium on Computer Architecture ISCA '90**, Volume 18 Issue 3a

Publisher: ACM Press

Full text available: pdf(1.19 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents an empirical evaluation of two memory-efficient directory methods for maintaining coherent caches in large shared memory multiprocessors. Both directory methods are modifications of a scheme proposed by Censier and Feautrier [5] that does not rely on a specific interconnection network and can be readily distributed across interleaved main memory. The schemes considered here overcome the large amount of memory required for tags in the original scheme in two different ways ...

16 The performance impact of flexibility in the Stanford FLASH multiprocessor

Mark Heinrich, Jeffrey Kuskin, David Ofelt, John Heinlein, Joel Baxter, Jaswinder Pal Singh, Richard Simoni, Kourosh Gharachorloo, David Nakahira, Mark Horowitz, Anoop Gupta, Mendel Rosenblum, John Hennessy

November 1994 **ACM SIGPLAN Notices , ACM SIGOPS Operating Systems Review , Proceedings of the sixth international conference on Architectural support for programming languages and operating systems ASPLOS-VI**, Volume 29 , 28 Issue 11 , 5

Publisher: ACM Press

Full text available: pdf(1.43 MB) Additional Information: full citation, abstract, references, citings, index terms

A flexible communication mechanism is a desirable feature in multiprocessors because it allows support for multiple communication protocols, expands performance monitoring capabilities, and leads to a simpler design and debug process. In the Stanford FLASH multiprocessor, flexibility is obtained by requiring all transactions in a node to pass through a programmable node controller, called MAGIC. In this paper, we evaluate the performance costs of flexibility by comparing the performance of ...

17 The evolution of the DECsystem 10

C. G. Bell, A. Kotok, T. N. Hastings, R. Hill

January 1978 **Communications of the ACM**, Volume 21 Issue 1

Publisher: ACM Press

Full text available: pdf(1.92 MB) Additional Information: full citation, abstract, references, citings, index terms

The DECsystem 10, also known as the PDP-10, evolved from the PDP-6 (circa 1963) over five generations of implementations to presently include systems covering a price range of five to one. The origin and evolution of the hardware, operating system, and languages are described in terms of technological change, user requirements, and user developments. The PDP-10's contributions to computing technology include: accelerating the transition from batch oriented to time sharing computing systems; ...

Keywords: architecture, computer structures, operating system, timesharing

18 Parallel approaches to short range molecular dynamics simulations

Pablo Tamayo, Jill P. Mesirov, Bruce M. Boghosian

August 1991

Proceedings of the 1991 ACM/IEEE conference on Supercomputing

Publisher: ACM Press

Full text available: pdf(818.30 KB) Additional Information: full citation, references, citings, index terms

19 Hardware acceleration of gate array layout

Philip M. Spira, Carl Hage

June 1985 **Proceedings of the 22nd ACM/IEEE conference on Design automation**

Publisher: ACM Press

Full text available: pdf(823.07 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we describe the hardware and software of a system which we have implemented to accelerate the physical design of gate arrays. In contrast to nearly all other reported approaches, our approach to hardware acceleration is to augment a single-user host workstation with a general-purpose microprogrammable slave processor having a large private memory. One or more such slaves can be attached. We have implemented placement improvement on the system, achieving a 20 x speedup vs. a hi ...

20 Curriculum '78: recommendations for the undergraduate program in computer science— a report of the ACM curriculum committee on computer science

Richard H. Austing, Bruce H. Barnes, Della T. Bonnette, Gerald L. Engel, Gordon Stokes

March 1979 **Communications of the ACM**, Volume 22 Issue 3

Publisher: ACM Press

Full text available: pdf(2.20 MB) Additional Information: full citation, abstract, references, citings

Contained in this report are the recommendations for the undergraduate degree program in Computer Science of the Curriculum Committee on Computer Science (C3S) of the Association for Computing Machinery (ACM). The core curriculum common to all computer science undergraduate programs is presented in terms of elementary level topics and courses, and intermediate level courses. Elective courses, used to round out an undergraduate program, are then discussed, and ...

Keywords: computer science curriculum, computer science education, computer science undergraduate degree programs, computer sciences courses, continuing education, service courses

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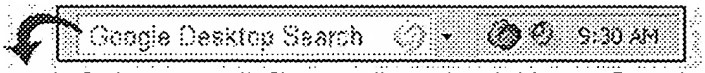

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A Parallel Architecture for Non-Deterministic Discrete Event Simulation
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D Keane - The University of Queensland, Department of Computer Science ..., 1999 - innovexpo.itee.uq.edu.au
... actual robots are constructed to maximize **acceleration** and mobility ... RS-232 data format
uses two **states** to ... transmitted using this **system** has the following format ...
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Parallel Logic **Simulation** of VLSI Systems
RD Chamberlain - DAC, 1995 - portal.acm.org
... uses pipelining techniques to **accelerate** the simula ... has clearly dominated parallel **simulation** research is ... accomplished via circulating **marker** algorithms that ...
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A Ferscha, SK Tripathi - 1994 - cs.nott.ac.uk
... Categories and Subject Descriptors: C.1.0 **Processor** Architectures:] General ... in terms of a set of **states** and events ... Performing a **simulation** thus means mimicking ...
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Parallel Logic **Simulation** of VLSI Systems
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... available in the VLSI system to **accelerate** the logic ... In discrete-eent **simulation**, system state variables are modeled ... and gate-level simulators add **states** to rem ...
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Modeling and **simulation** of the Automated Highway System
FH Eskafi, P Varaiya - 1996 - path.berkeley.edu
... and Housing Agency, Department of Transportation; and the United **States** Department of ... 4.2 Distributed **Simulation** of Hybrid System ... 4.2.1 The **Processor** Model . ...
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... under the aegis of the United **States** Department ... the proposed **simulation** architecture is examined in Section 5.2. ... which are applied to **accelerate** the simulator. ...
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[PS] ... and Experimental Evaluation of a Scalable Multiprocessor Architecture for Qualitative **Simulation**
D der Technischen Wissenschaften - iti.tu-graz.ac.at
... **processor** system consisting of digital signal processors TMS320C40 ... The **simulation** process in the device-oriented approach ... the set of all possible **states** of the ...
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SCIENTIFIC **SIMULATION** INITIATIVE
E Summary - fusion.gat.com
... equation in time by advancing **marker**-particles along ... be cost-effective, it must **accelerate** as large ... be addressed with particle **simulation** techniques analogous ...
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A Roth, GS Sohi - HPCA, 2001 - doi.ieeecomputersociety.org
... accurate estimates require detail equivalent to full **simulation**. ... matching address/identifier pair (**marker** 8 ... a data-driven multithreading enabled SMT **processor**. ...
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Adapted Unstructured LBM for Flow **Simulation** on Curved Surfaces
Z Fan, Y Zhao, A Kaufman, Y He - Proceedings of the 2005 ACM SIGGRAPH/Eurographics symposium ..., 2005 - portal.acm.org
... Figure 4). In the **simulation**, for each time-step we first up- date the **states** of all ghost points based on corresponding neighboring points, and then for each ...

Web Search - cs.sunysb.edu - portal.acm.org

Worst Case Execution Time Estimation for Advanced **Processor** Architectures
L fur Realzeit–Computersysteme - deposit.ddb.de
... in some cases the coding guidelines even **accelerate** the code ... may be executed through the **marker** within one ... publication [65] focusses on the **simulation** of caches ...
Web Search - tumb1.biblio.tu-muenchen.de - cs.york.ac.uk - www-users.cs.york.ac.uk

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L3	20	((kernel with mode) with (thread or process)) and simulat$5 and ((signal with patterns) or stimulus or (test adj bench))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/02 12:28
L4	15	(worker adj thread) and simulat$5 and ((signal with patterns) or stimulus or (test adj bench))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/02 12:30
L5	137	(accel$8 and simulation).ti.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/02 12:32
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L9	330	(accelerator or acceleration) and (simulation or simulator) and (accelerated with process)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/02 12:41

L10	1	9 and simulator.ti.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/02 12:42
L11	657	(703/22).CCLS.	US-PGPUB; USPAT	OR	OFF	2005/12/02 12:42
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L13	39	11 and accel$6	US-PGPUB; USPAT	OR	ON	2005/12/02 12:57
L14	1	("6336087").PN.	USPAT	OR	OFF	2005/12/02 12:59
L15	366	11 not 13	USPAT	OR	OFF	2005/12/02 12:59